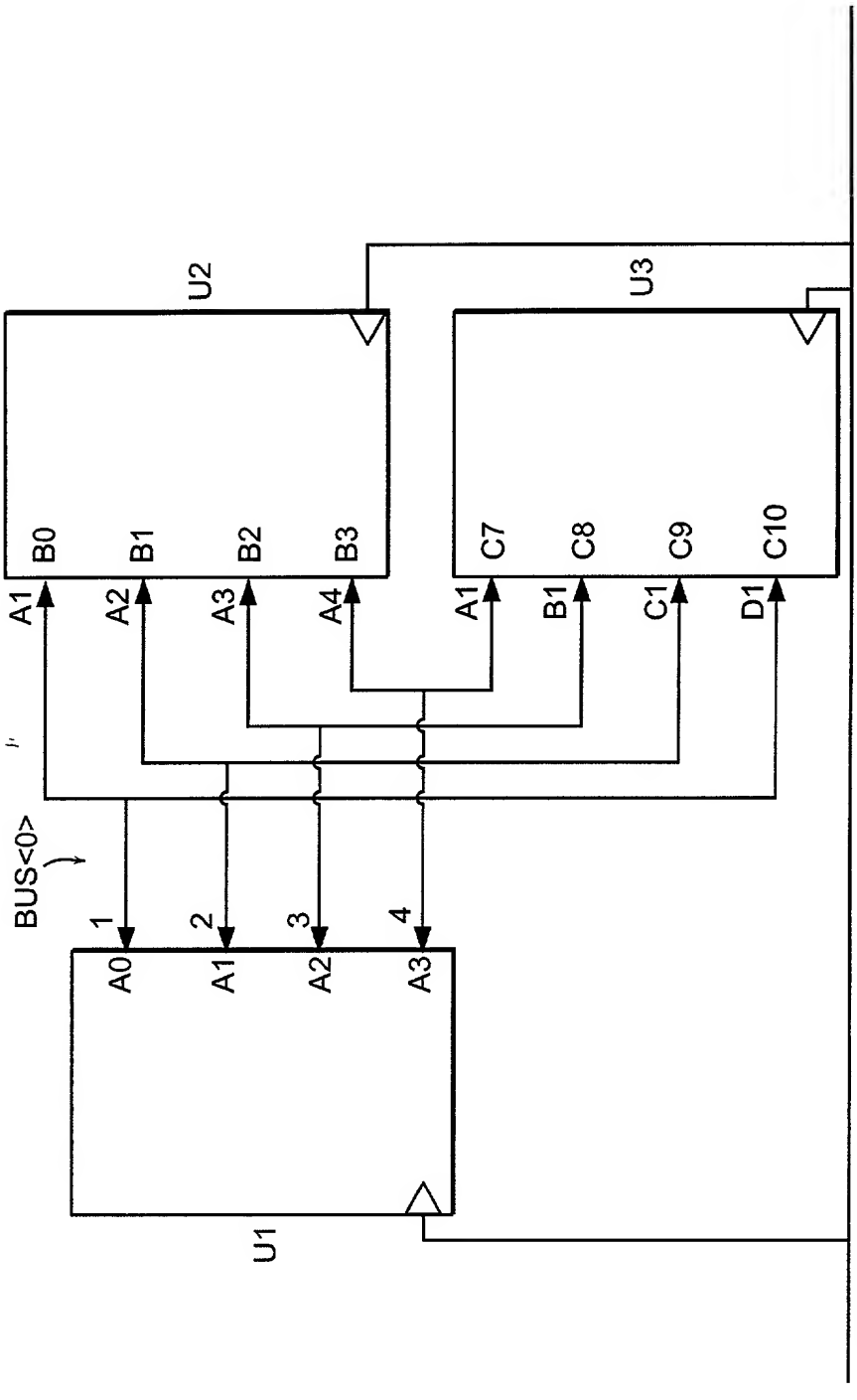

FIG. 1
PRIOR ART

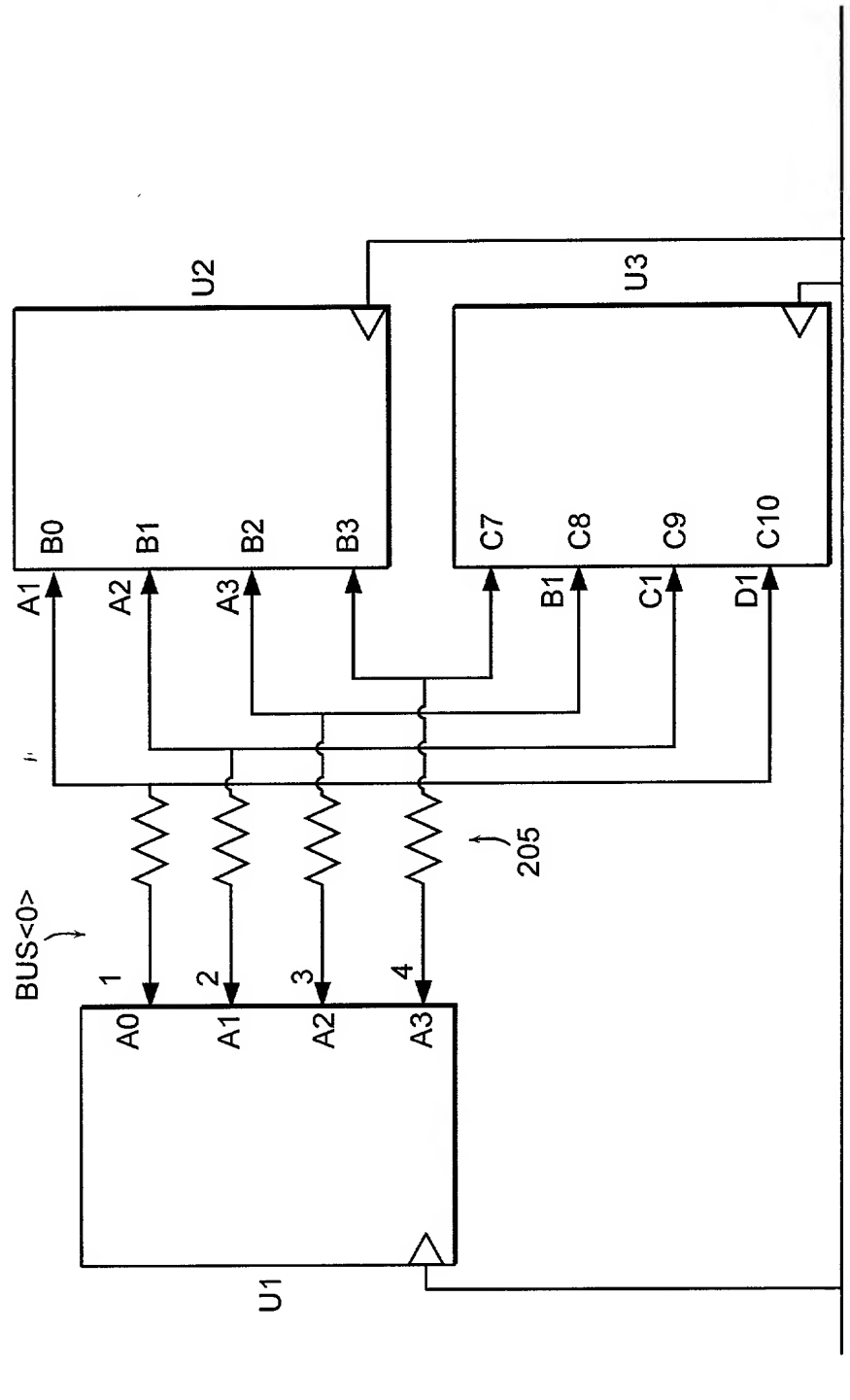

FIG. 2
PRIOR ART

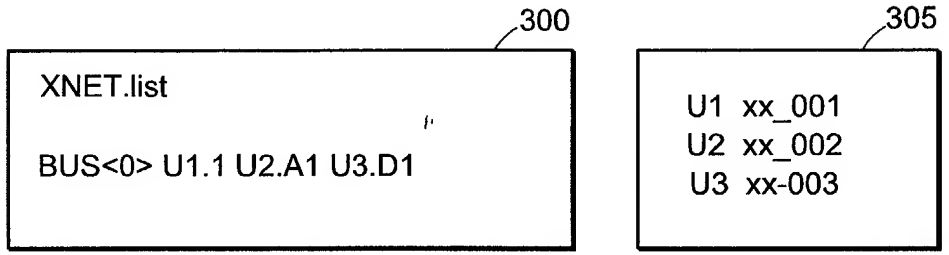

FIG. 3
PRIOR ART

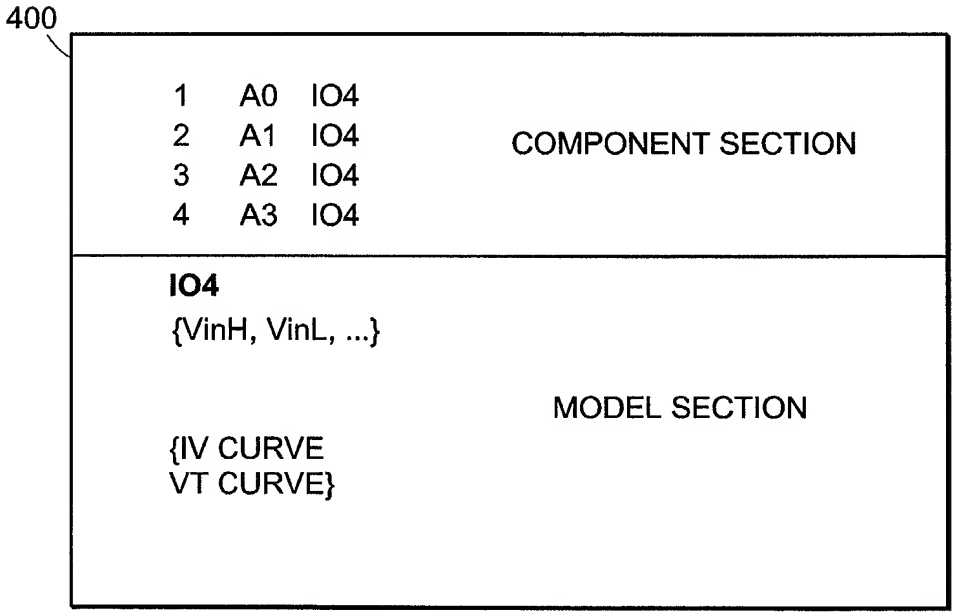

FIG. 4
PRIOR ART

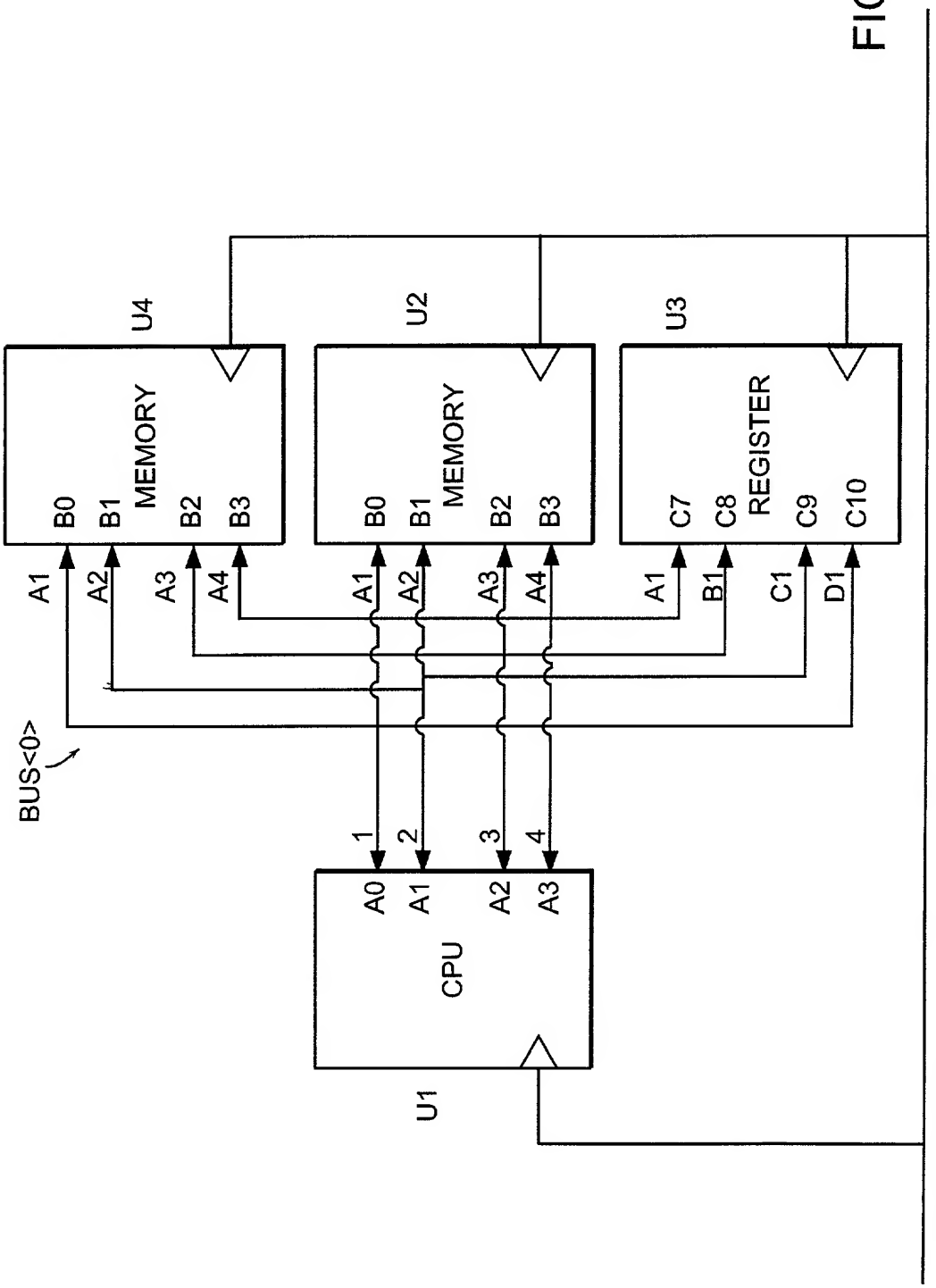
U4
MEMORY
B0
B1
B2
B3
U2
MEMORY
B0
B1
B2
B3
U3
REGISTER
C7
C8
C9
C10
A1
A2
A3
A4
A1
A2
A3
A4
A1
B1
C1
D1
BUS<0>
1
2
3
4
U1
CPU
A0
A1
A2
A3
CLOCK SIGNAL

FIG. 5

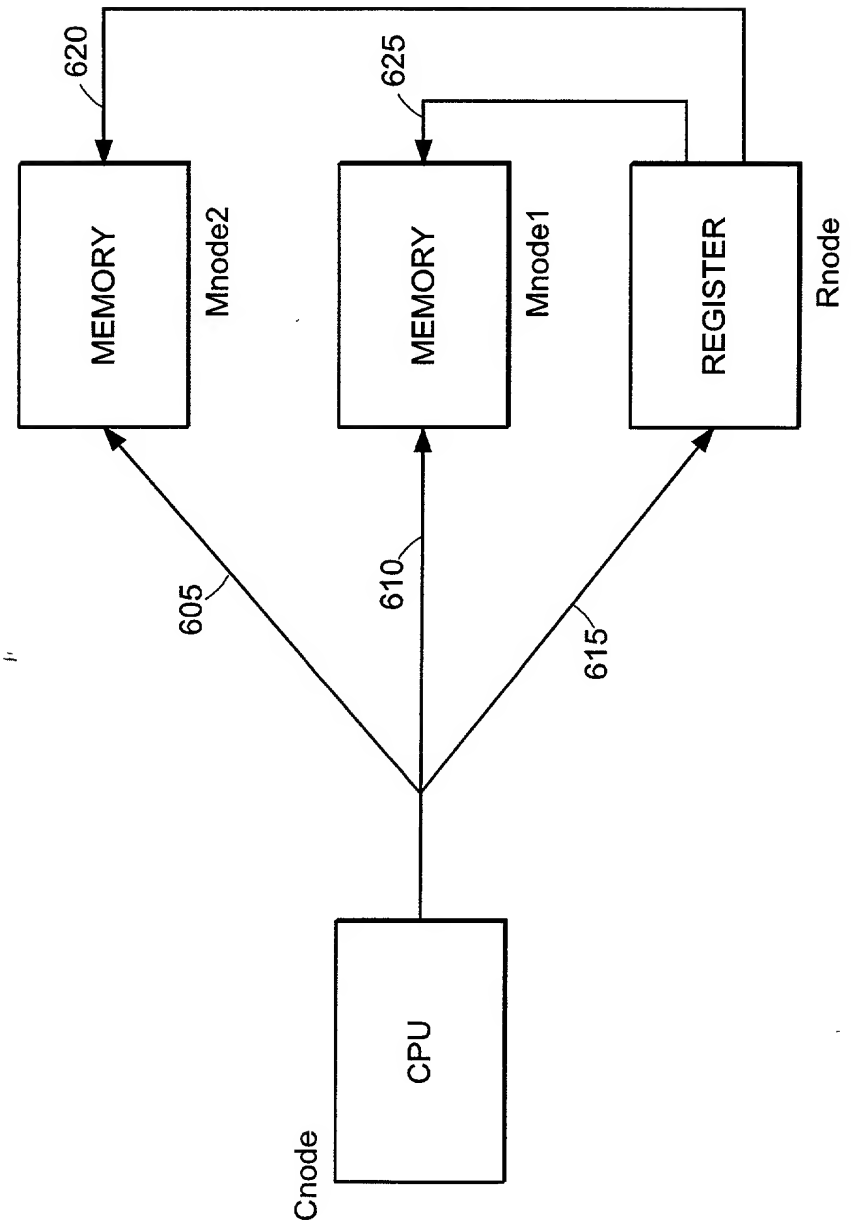
620
625
MEMORY
Mnode2
MEMORY
Mnode1
REGISTER
Rnode
605
610
615
CPU
Cnode

FIG. 6

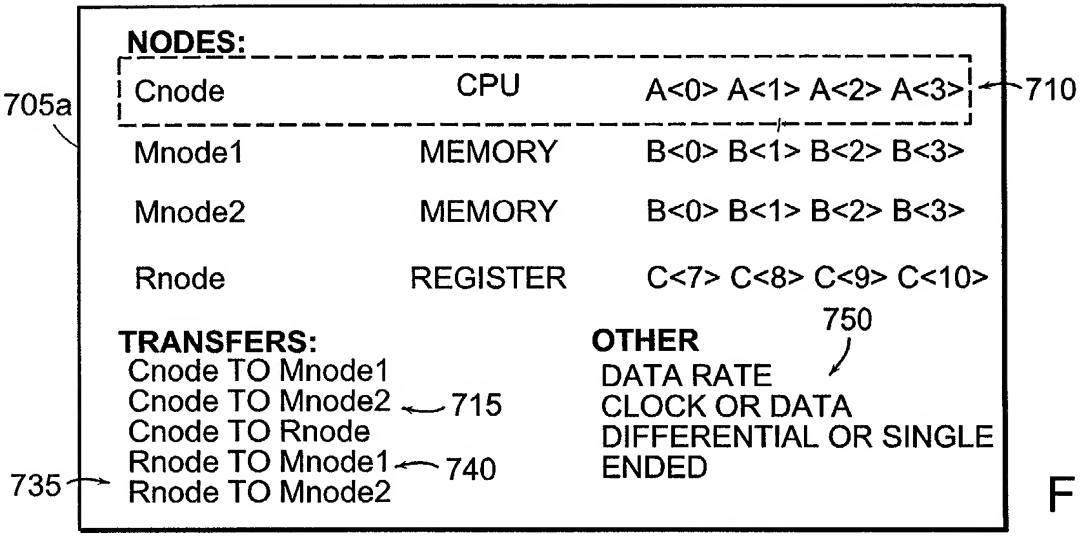
NODES:
Cnode CPU A<0> A<1> A<2> A<3>
Mnode1 MEMORY B<0> B<1> B<2> B<3>
Mnode2 MEMORY B<0> B<1> B<2> B<3>
Rnode REGISTER C<7> C<8> C<9> C<10>
TRANSFERS:
Cnode TO Mnode1
Cnode TO Mnode2
Cnode TO Rnode
Rnode TO Mnode1
Rnode TO Mnode2
OTHER
DATA RATE
CLOCK OR DATA
DIFFERENTIAL OR SINGLE ENDED
705a
710
715
740
735
750

FIG. 7A

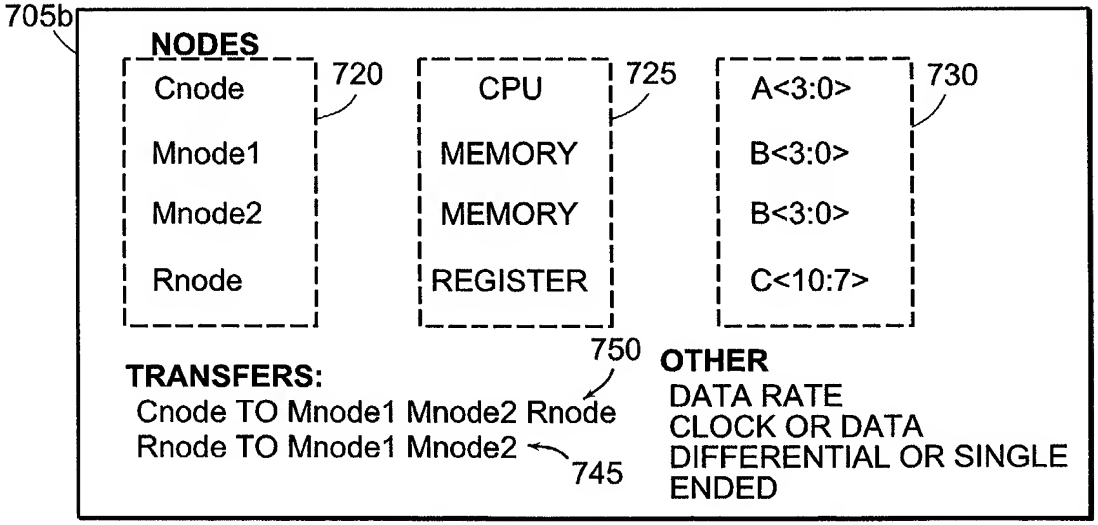
NODES
Cnode
Mnode1
Mnode2
Rnode
CPU
MEMORY
MEMORY
REGISTER
A<3:0>
B<3:0>
B<3:0>
C<10:7>
TRANSFERS:
Cnode TO Mnode1 Mnode2 Rnode
Rnode TO Mnode1 Mnode2
OTHER
DATA RATE
CLOCK OR DATA
DIFFERENTIAL OR SINGLE ENDED
705b
720
725
730
745
750

FIG. 7B

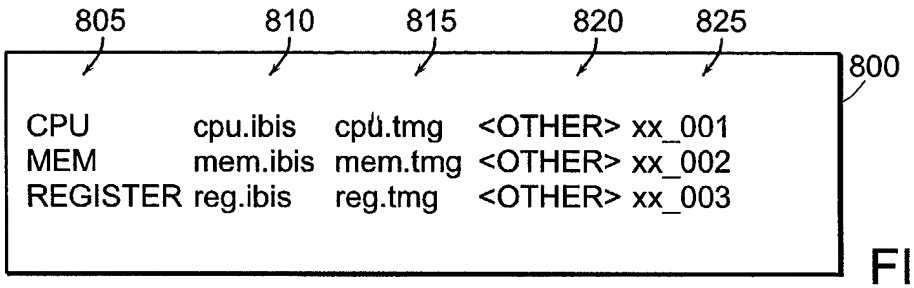
805
810
815
820
825
800
CPU cpu.ibis cpu.tmg <OTHER> xx_001
MEM mem.ibis mem.tmg <OTHER> xx_002
REGISTER reg.ibis reg.tmg <OTHER> xx_003

FIG. 8

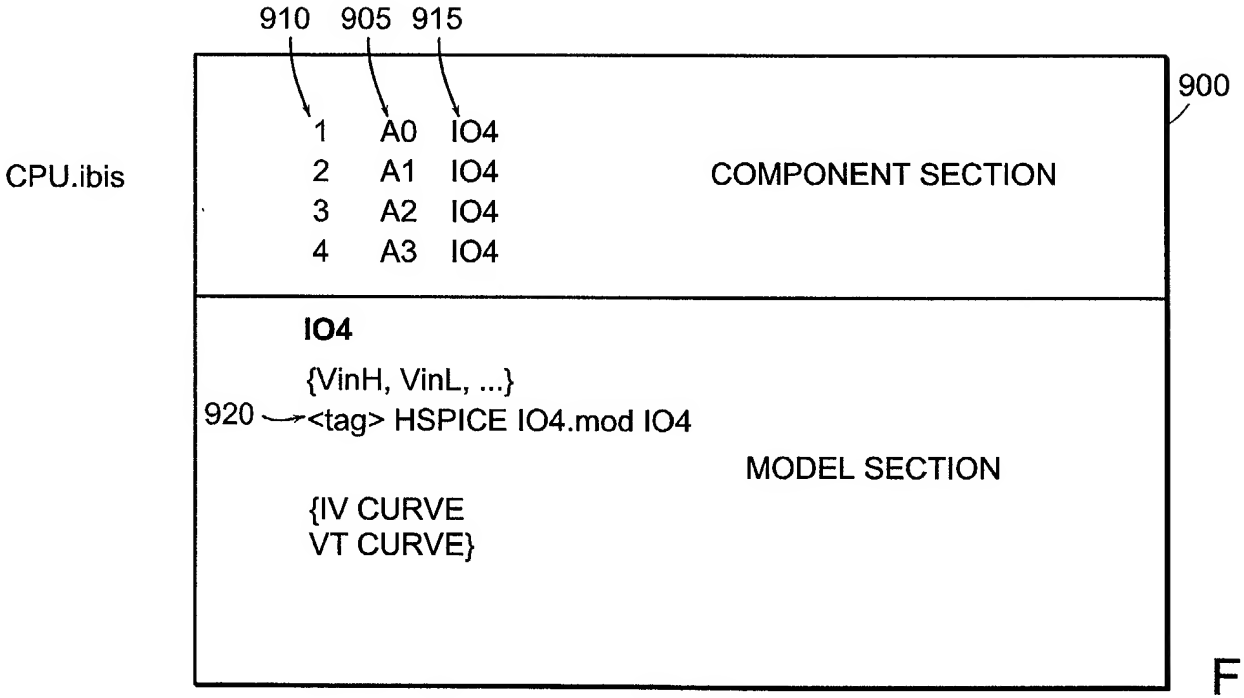
910
905
915
900
CPU.ibis
1 A0 IO4
2 A1 IO4
3 A2 IO4
4 A3 IO4
COMPONENT SECTION
IO4
{VinH, VinL, ...}
920
<tag> HSPICE IO4.mod IO4
MODEL SECTION
{IV CURVE
VT CURVE}

FIG. 9

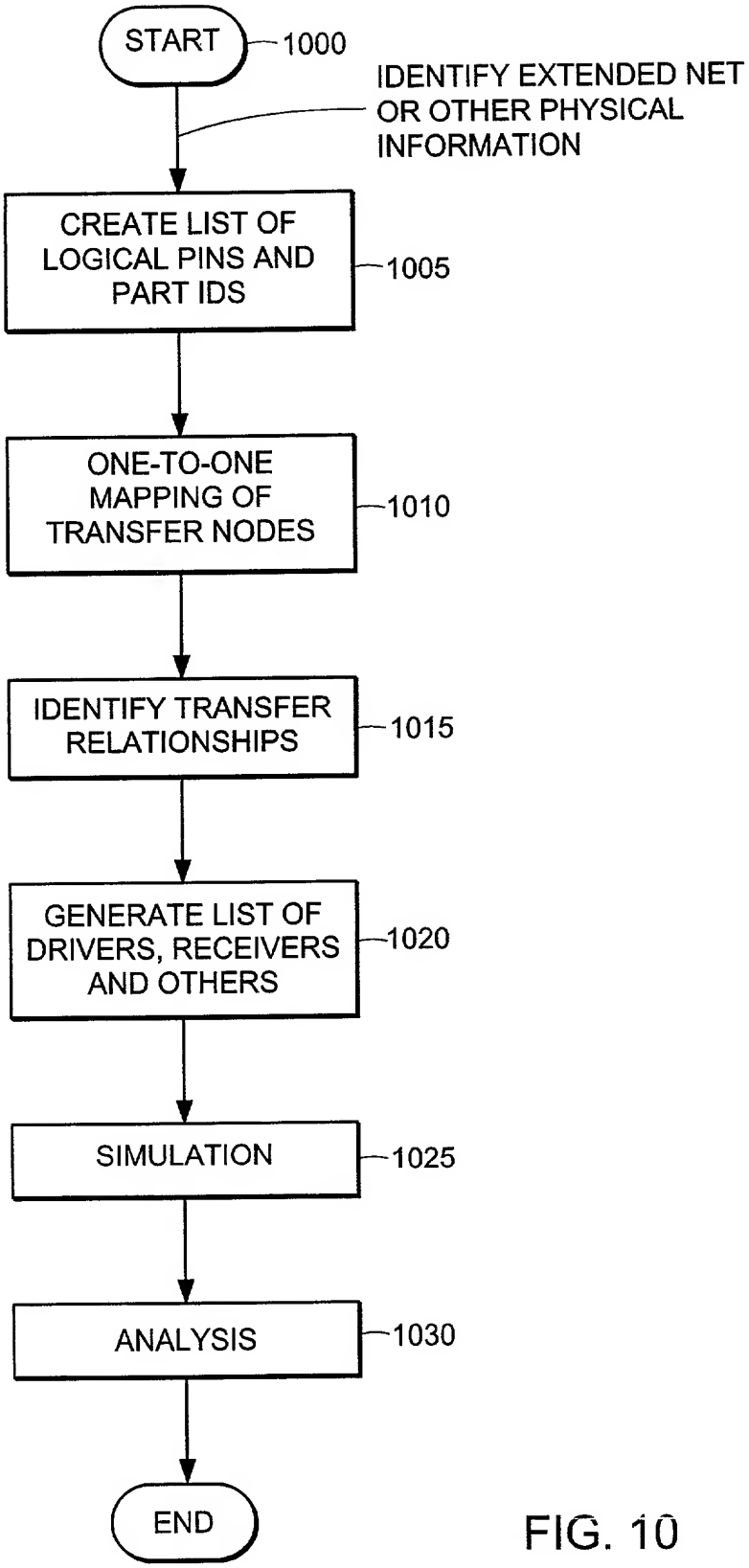
START
1000
IDENTIFY EXTENDED NET OR OTHER PHYSICAL INFORMATION
CREATE LIST OF LOGICAL PINS AND PART IDS
1005
ONE-TO-ONE MAPPING OF TRANSFER NODES
1010
IDENTIFY TRANSFER RELATIONSHIPS
1015
GENERATE LIST OF DRIVERS, RECEIVERS AND OTHERS
1020
SIMULATION
1025
ANALYSIS
1030
END

FIG. 10

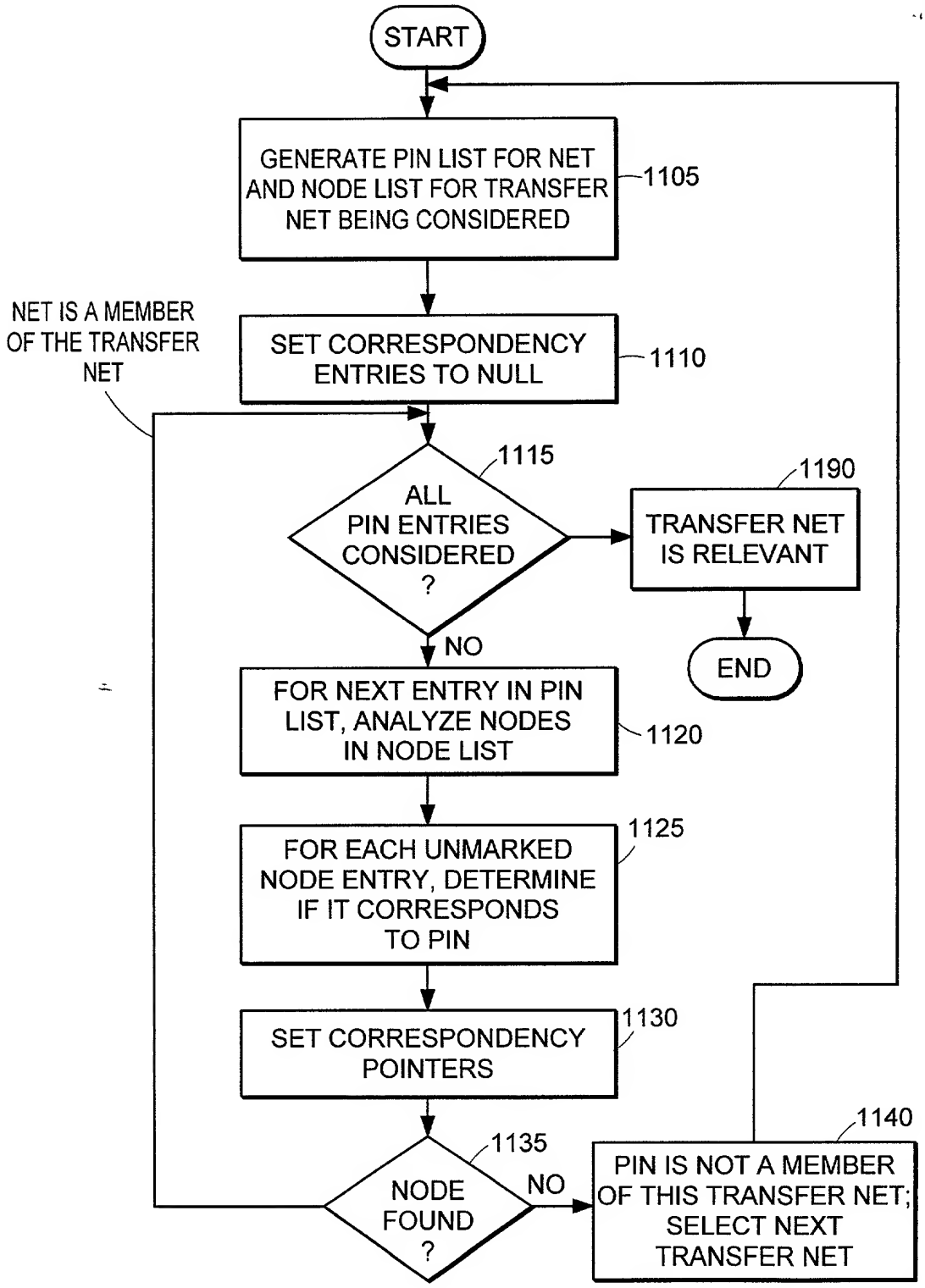
START
GENERATE PIN LIST FOR NET AND NODE LIST FOR TRANSFER NET BEING CONSIDERED
1105
NET IS A MEMBER OF THE TRANSFER NET
SET CORRESPONDENCY ENTRIES TO NULL
1110
1115
ALL PIN ENTRIES CONSIDERED ?
1190
TRANSFER NET IS RELEVANT
END
NO
FOR NEXT ENTRY IN PIN LIST, ANALYZE NODES IN NODE LIST
1120
FOR EACH UNMARKED NODE ENTRY, DETERMINE IF IT CORRESPONDS TO PIN
1125
SET CORRESPONDENCY POINTERS
1130
1135
NODE FOUND ?
NO
1140
PIN IS NOT A MEMBER OF THIS TRANSFER NET; SELECT NEXT TRANSFER NET

FIG. 11

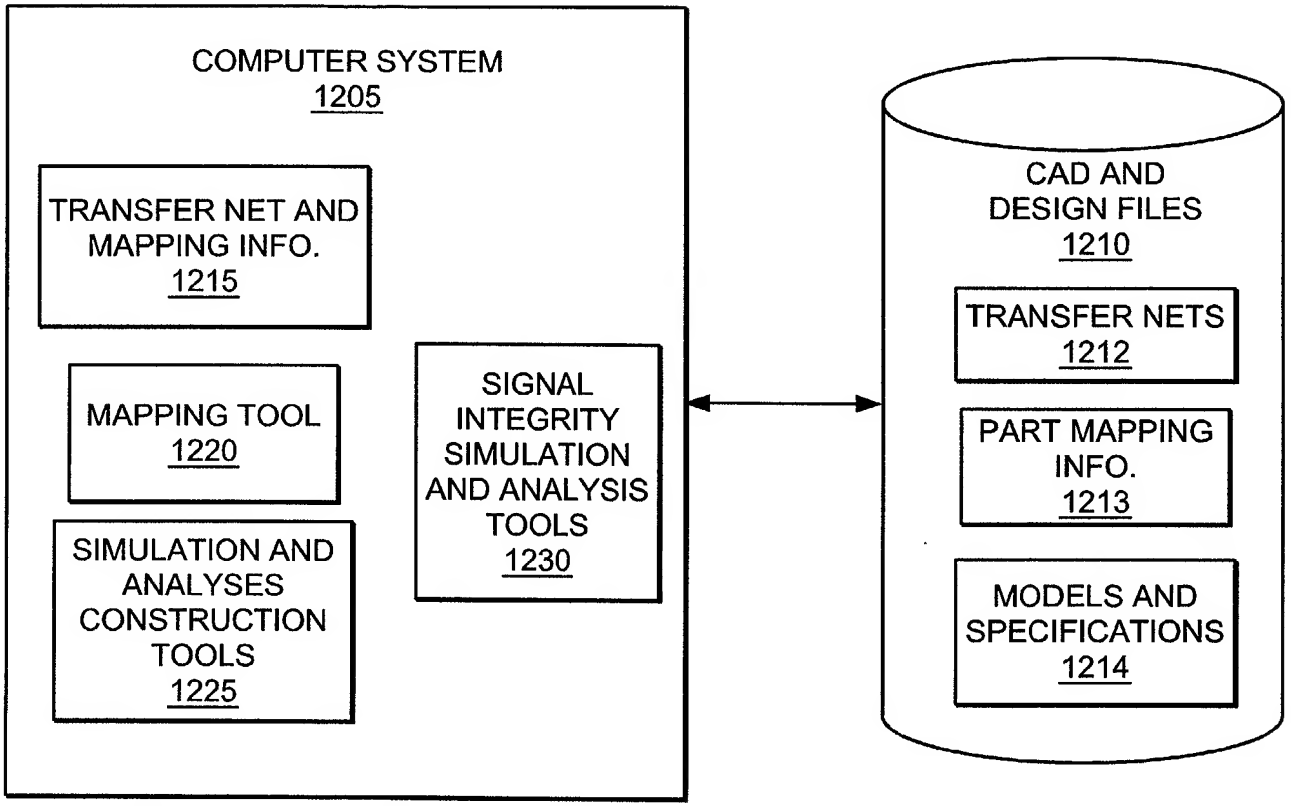
COMPUTER SYSTEM
1205
TRANSFER NET AND MAPPING INFO.
1215
MAPPING TOOL
1220
SIMULATION AND ANALYSES CONSTRUCTION TOOLS
1225
SIGNAL INTEGRITY SIMULATION AND ANALYSIS TOOLS
1230
CAD AND DESIGN FILES
1210
TRANSFER NETS
1212
PART MAPPING INFO.
1213
MODELS AND SPECIFICATIONS
1214

FIG. 12